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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,458	10/29/2003	Abbas Amirichimeh	1875.3640002/JTH/TAD	4577

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1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER

JAIN, RAJ K

ART UNIT	PAPER NUMBER
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2616

MAIL DATE	DELIVERY MODE
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05/16/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/695,458

Applicant(s)

AMIRICHIMEH ET AL.

Examiner

Raj K. Jain

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5, 7-13, 17-25, 37-43 and 2935 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7-13, 17, 24, 25, 29-36, 41 and 42 is/are rejected.
- 7) ☒ Claim(s) 18-23, 37-40 and 43 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>5/8/07</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-5, 7-13, 17-25, 29-35, 37-43 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. With respect to claims 1, 7, 13, 17, 30, 32, and 41, the claims recite a transmission of a "signal" from a source to destination. According to MPEPE 2106.01 [R-5] here in part;

"When nonfunctional descriptive material is recorded on some computer-readable medium, in a computer or on an electromagnetic carrier signal, it is not statutory since no requisite functionality is present to satisfy the practical application requirement.

The "signal" presented in subject claims is simply an "electromagnetic signal" with no practical utility, and therefore making the claims non-statutory.

Claims, 4-5, 8-13, 18-25, 29, 31, 33-35, 37-40, 42, and 43 are also rejected based on their dependency to a rejected base claim.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 10, 11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The subject claims recite here in part "...delay buffers to be configured one of to convey said first bit through said delay buffer and to bypass said first bit around said delay buffer". The language is vague and confusing, it is not clear from the specification or drawings whether the "first bit" is being conveyed or bypassed. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 13, 17, 24, 25, 29, and 32-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Champlin et al (USP 4,627,070).

Regarding claims 1, 13, 17, 24, and 32, Champlin discloses a cross link multiplexer bus (see Figs. 1, 9, 17), comprising:

a plurality of cross link multiplexers MT1, MT2,(see Fig. 9), said plurality of cross link multiplexers having a destination port configured to receive a signal and an origin

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port configured to produce said signal (Each MT has origin port and destination port, for example MT1 has origin port at 10a and destination port at 10b); and

a plurality of interconnects (10a, 10b), wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers (see Fig. 9, 10a and 10b interconnects are between respective cross link multiplexers);

wherein a first interconnect of said set of interconnects has a first length, a second interconnect of said set of interconnects has a second length, and said first length and said second length are substantially equal (see col 8 lines 60-67, lengths of MTs are arbitrary and therefore can be of equal length if so desired);

wherein said first interconnect is configured to convey a first bit of a number of bits and said second interconnect is configured to convey a second bit of said number of bits and said first bit remains substantially synchronized with said second bit (see col 6 lines 39-52, Fig. 4 col 8 lines 24-52, messages and therefore digital pulses or bits are synchronized prior to transmission).

Regarding claims 2 and 3, Champlin discloses a circular configuration, other configurations are possible based on user preferences (see Fig. 9, col 4 lines 20-45).

Regarding claim 4, Champlin discloses pair of cross-link multiplexers (see Fig. 9, col 12 lines 45-50.).

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Regarding claim 5, Champlin discloses message and/or data transmission, a message or data inherently incorporates "characters" and bits (see abstract, and general spec.).

Regarding claims 25, 29, 33 and 35 Champlin discloses plurality of multiplexers configured to receive and/or transmit signals (see Fig. 9).

Regarding claim 34 Champlin discloses format conversion (see col 6 lines 45-51.).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 7-12, 30, 31, 41 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Champlin et al (USP 4,627,070) in view of Schoner et al (USP 6,137,734).

Regarding claims 7, 30 and 41, Champlin discloses a cross link multiplexer bus (see Figs. 1, 9, 17), comprising:

a plurality of cross link multiplexers MT1, MT2,(see Fig. 9), said plurality of cross link multiplexers having a destination port configured to receive a signal and an origin port configured to produce said signal (Each MT has origin port and destination port, for example MT1 has origin port at 10a and destination port at 10b); and

a plurality of interconnects (10a, 10b), wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers (see Fig. 9, 10a and 10b interconnects are between respective cross link multiplexers);

wherein a first interconnect of said set of interconnects has a first length, a second interconnect of said set of interconnects has a second length, and said first length and said second length are substantially equal (see col 8 lines 60-67, lengths of MTs are arbitrary and therefore can be of equal length if so desired);

wherein said first interconnect is configured to convey a first bit of a number of bits and said second interconnect is configured to convey a second bit of said number of bits and said first bit remains substantially synchronized with said second bit (see col 6 lines 39-52, Fig. 4 col 8 lines 24-52, messages and therefore digital pulses or bits are synchronized prior to transmission).

Champlin fails to disclose a delay buffer.

Schoner discloses a delay buffer (see col 3 lines 35 – col 4 line 25.). A delay buffer within a communications network provides a synchronized timing to improve the speed and reliability of communications systems.

Thus it would have been obvious at the time the invention was made to incorporate the teachings of Schoner within Champlin so as to improve the speed and reliability of communications systems.

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Regarding claim 8, Champlin discloses message and/or data transmission, a message or data inherently incorporates “characters” and bits (see abstract, and general spec.).

Regarding claims 9-11, 31, 42, Schoner discloses a series of delay buffers which respectively convey a bit (see Fig. 3b), reasons for combining are same as for claim 7.

Regarding claims 12, Schoner discloses delay buffers (see Fig. 3b, col 3 lines 35 – col 4 line 25.), within a communications network which provides a “synchronized” timing to improve the speed and reliability of communications systems.

Allowable Subject Matter

Claims 18-23, 37-40 and 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Raj K. Jain whose telephone number is 571-272-3145. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Raj K. Jain

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May 10, 2007